Notice of References Cited	Application/Control No. 10/812,141	Applicant(s)/Patent Under Reexamination BARRACK ET AL.	
	Examiner Thong H. Vu	Art Unit 2619	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,667,744 B2	12-2003	Buckelew et al.	345/502
*	B	US-7,215,666 B1	05-2007	Beshai et al.	370/380
*	C	US-2004/0120349 A1	06-2004	Border et al.	370/474
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	A 110 nm 512 Mb DDR DRAM with vertical transistor trench cell Wuensche, S.; VLSI Circuits Digest of Technical Papers, 2002. Symposium on 13-15 June 2002 Page(s):114 - 115
	V	Design of the high-speed, high-precision and large-scale data acquisition system Hou Xiaomin; Wang Xiaohong; Long Teng; Signal Processing, 2004. Proceedings. ICSP '04. 2004 7th International Conference on Volume 1, 31 Aug.-4 Sept. 2004 Page(s):563 - 566 vol.1
	W	Adaptable ferroelectric memories for space applications Kamp, D.A.; DeVilbiss, A.D.; Philpy, S.C.; Derbenwick, G.F., Non-Volatile Memory Technology Symposium, 2004 15-17 Nov. 2004 Page(s):149 - 152
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.